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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/822,052	03/30/2001	Sanjay Ramakrishna Pillay	1138-EP	8450

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EXAMINER	
CHU, GABRIEL L	
ART UNIT	**PAPER NUMBER**
2184	4

DATE MAILED: 11/26/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/822,052	Applicant(s) PILLAY ET AL.	
	Examiner Gabriel L. Chu	Art Unit 2184	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 March 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *8 and 10-13* is/are allowed.

6)☒ Claim(s) *1-6,16 and 17* is/are rejected.

7)☒ Claim(s) *7,9,14,15 and 18-20* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Objections

1. Claims 9, 14, 15, and 16 are objected to because of the following informalities:

Referring to claim 9, "the selected one of the memories" is understood to refer to "a selected one of the memories", correcting for antecedence.

Referring to claims 14 and 15, both claims refer to "said second processor" which is introduced in claim 13. For the purpose of examination, claims 14 and 15 are each understood to depend from claim 13 instead of claim 8.

Referring to claim 16, "the selected triggering parameters" is understood to refer to "the selected triggering event parameters", correcting for antecedence.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

3. Claims 1-6, 16, and 17 are rejected under 35 U.S.C. 102(a) as being anticipated by US 6131174 to Fischer et al. Referring to claim 1, Fischer et al. disclose a debug subsystem for testing a system-on-a-chip including an embedded processor and memory (From the abstract, "An interlocutor system and method is described that allows for at-speed testing of an embedded microcontroller at the control of an embedded digital signal processor in a system-on-a-chip architecture. The interlocutor

system includes a buffer for temporarily storing test program data words output by the DSP and retrieved by the microcontroller being tested and a control circuit for controlling the microcontroller and DSP. The microcontroller, DSP, and interlocutor system are all located on a single integrated circuit.") comprising: at least one sub-block operable to: monitor a bus between the processor and the memory to detect selected triggering events, count the number of triggering events detected (From line 22 of column 2, "In preferred embodiments, the control circuit comprises a counter which is incremented when a data word is latched into the buffer and decremented when a data word is retrieved from the buffer by the microcontroller. The counter is initialized to zero so that when the buffer is empty, the counter is empty."); and when the number of triggering events reaches a predetermined threshold, generating a debugging signal (From line 27 of column 2, "When the counter is empty, the microcontroller clock is disabled so the microcontroller is prevented from attempting to retrieve any data from the buffer.").

Referring to claim 2, Fischer et al. disclose the triggering events comprise memory accesses (From line 22 of column 2, "In preferred embodiments, the control circuit comprises a counter which is incremented when a data word is latched into the buffer and decremented when a data word is retrieved from the buffer by the microcontroller. The counter is initialized to zero so that when the buffer is empty, the counter is empty.").

Referring to claim 3, Fischer et al. disclose the memory accesses are selected from the group including reads and writes (From line 22 of column 2, "In preferred embodiments, the control circuit comprises a counter which is incremented when a data

word is latched into the buffer and decremented when a data word is retrieved from the buffer by the microcontroller. The counter is initialized to zero so that when the buffer is empty, the counter is empty.").

Referring to claim 4, Fischer et al. disclose the triggering events comprise memory accesses within a selected address range (From line 28 of column 4, "The counter 44 is an up/down counter corresponding to the depth of the data latch 42 and having an EMPTY flag which is set when the counter 44 is at zero and a FULL flag which is set when the counter is at a maximum value corresponding to a full data latch 42. If the data latch 42 has a one data word capacity, the counter 44 may be a toggle flip-flop which assumes two states-one state, the EMPTY state, when the data latch is empty and capable of receiving a data word from the DSP 14, and another state, the FULL state, when the data latch 42 contains a data word ready to be retrieved by the microprocessor 12. If the data latch 42 has a multi-data word capacity, the counter 44 has a number of bits required for counting the number of data words which may be stored in the data latch 42." Wherein memory accesses occur within the range dictated by latch capacity.).

Referring to claim 5, Fischer et al. disclose the debugging signal is operable to freeze a clock timing the operation of the processor (From line 27 of column 2, "When the counter is empty, the microcontroller clock is disabled so the microcontroller is prevented from attempting to retrieve any data from the buffer.").

Referring to claim 6, Fischer et al. disclose the debugging signal comprises an interrupt to the processor (From line 27 of column 2, "When the counter is empty, the

microcontroller clock is disabled so the microcontroller is prevented from attempting to retrieve any data from the buffer." Wherein preventing the microcontroller from attempting to retrieve data interrupts the processor.).

Referring to claim 16, Fischer et al. disclose a method of debugging a single-chip system including an embedded processor and memory (From the abstract, "An interlocutor system and method is described that allows for at-speed testing of an embedded microcontroller at the control of an embedded digital signal processor in a system-on-a-chip architecture. The interlocutor system includes a buffer for temporarily storing test program data words output by the DSP and retrieved by the microcontroller being tested and a control circuit for controlling the microcontroller and DSP. The microcontroller, DSP, and interlocutor system are all located on a single integrated circuit.") comprising the steps of: selecting triggering event parameters, monitoring transactions between the processor and the memory to detect triggering events corresponding to the selected triggering event parameters, counting the number of triggering events detected (From line 22 of column 2, "In preferred embodiments, the control circuit comprises a counter which is incremented when a data word is latched into the buffer and decremented when a data word is retrieved from the buffer by the microcontroller. The counter is initialized to zero so that when the buffer is empty, the counter is empty."); and when the number of triggering events reaches a predetermined threshold, generating a debugging signal (From line 27 of column 2, "When the counter is empty, the microcontroller clock is disabled so the microcontroller is prevented from attempting to retrieve any data from the buffer.").

Referring to claim 17, Fischer et al. disclose said step of selecting triggering event parameters comprises the substeps of: selecting a triggering memory access type (From line 22 of column 2, "In preferred embodiments, the control circuit comprises a counter which is incremented when a data word is latched into the buffer and decremented when a data word is retrieved from the buffer by the microcontroller. The counter is initialized to zero so that when the buffer is empty, the counter is empty."); and selecting a triggering address range (From line 28 of column 4, "The counter 44 is an up/down counter corresponding to the depth of the data latch 42 and having an EMPTY flag which is set when the counter 44 is at zero and a FULL flag which is set when the counter is at a maximum value corresponding to a full data latch 42. If the data latch 42 has a one data word capacity, the counter 44 may be a toggle flip-flop which assumes two states-one state, the EMPTY state, when the data latch is empty and capable of receiving a data word from the DSP 14, and another state, the FULL state, when the data latch 42 contains a data word ready to be retrieved by the microprocessor 12. If the data latch 42 has a multi-data word capacity, the counter 44 has a number of bits required for counting the number of data words which may be stored in the data latch 42." Wherein memory accesses occur within the range dictated by latch capacity.).

Allowable Subject Matter

4. Claims 7 and 18-20 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Referring to claim 7, the prior

art, in light of the parent claim, does not teach or fairly suggest the triggering events comprise predetermined data values appearing on a data bus.

Referring to claim 18, the prior art, in light of the parent claim, does not teach or fairly suggest the memory comprises a plurality of memory spaces and said step of selecting triggering event parameters comprises the step of selecting one of the memory spaces for monitoring.

Referring to claim 19, the prior art, in light of the parent claim, does not teach or fairly suggest said step of monitoring comprises the step of monitoring an address bus to the memory for memory accesses meeting the triggering event parameters.

Referring to claim 20, the prior art, in light of the parent claim, does not teach or fairly suggest said step of selecting triggering event parameters comprises the step of selecting triggering events to step through code being run by the processor.

5. Claims 9, 14, and 15 are objected to as having objectionable matter, but would be allowable if rewritten to overcome the objectionable matter.

6. Claims 8 and 10-13 are allowed.

7. The following is an examiner's statement of reasons for allowance: Referring to claims 8 and 10-13, the prior art does not teach or fairly suggest a debug block comprising a plurality of independently programmable debug sub-blocks each for monitoring accesses to selected one of said memories and detecting triggering events, a system on a chip comprising: at least one processor; a plurality of memory spaces accessible by said processor via address and data buses; each subblock comprising: a first register for setting triggering event parameters; a second register for setting a

threshold number of triggering events; a counter for maintaining a count of detected triggering events; and circuitry for generating a control signal when the count reaches the threshold..

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

US 5321828 to Phillips et al.

US 5329471 to Swoboda et al., from line 42 of column 56, "1. Hardware breakpoints, qualification on memory write (MW), memory read (MR), instruction acquisition (IAQ), as well as address and data hardware breakpoints. The breakpoints are multiple or sequenced. An event counter 1715 of FIG. 64 provides a breakpoint on occurrence of a repeated occurante of a predetermined condition. A stop point is defined at a predetermined time after a breakpoint event has occurred."

US 5426741 to Butts, Jr. et al.

US 5687311 to Hasmimoto

US 5875294 to Roth et al.

US 5951696 to Naaseh et al.

US 6012142 to Dokic et al.

US 6587967 to Bates et al.

US 6601189 to Edwards et al.

"Debugging Aids for Systems-on-a-Chip" by Bannatyne

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Gabriel L. Chu whose telephone number is (703) 308-7298. The examiner can normally be reached on weekdays with alternate Fridays off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert W. Beausoliel, Jr. can be reached on (703) 305-9713. The fax phone number for the organization where this application or proceeding is assigned is (703) 746-7239.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

gc

SCOTT BADERMAN
PRIMARY EXAMINER